

Design of a Clock Distribution Network (CDN) as an H-Tree

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Abstract—This project presents the design and simulation of a Clock Distribution Network (CDN) using an H-Tree architecture. The H-Tree was modeled using the Keysight Advanced Design System (ADS) to achieve balanced clock signal propagation with minimal skew across sixteen endpoints. LineCalc was used to calculate interconnect parameters that yield a target impedance of 45Ω , ensuring impedance matching and minimizing reflections. Both ideal and physical transmission line models were implemented—ideal lossless TLIN lines and physical MLIN/SLIN structures with defined substrate properties. Transient simulation results confirmed symmetrical waveform propagation and minimal skew (<12 ps) among the outputs. These findings validate the use of symmetric H-Tree structures for robust, low-skew clock distribution in high-frequency systems.

Index Terms—Clock Distribution Network, H-Tree, LineCalc, ADS Simulation, Transmission Lines, Clock Skew, Microstrip, Stripline

I. INTRODUCTION

High-performance digital systems require precise synchronization of clock signals distributed to multiple functional blocks. Even nanosecond-level mismatches in clock arrival times can lead to logic timing violations and data corruption. This mismatch, known as clock skew, results from differences in interconnect length, impedance, and propagation delay along the distribution network. As clock frequencies continue to rise into the gigahertz range, minimizing skew has become one of the most critical aspects of integrated circuit (IC) design.

To address these challenges, various clock distribution topologies have been developed, including clock spines, grids, and tree-based networks. Among these, the H-Tree architecture has proven particularly effective for balanced distribution because of its geometrical symmetry. Each branch of an H-Tree splits into two identical paths, ensuring that all endpoints are equidistant from the source. This symmetrical structure theoretically eliminates skew in an ideal lossless system, making it the preferred topology for high-speed microprocessors and field-programmable gate arrays (FPGAs).

The effectiveness of an H-Tree, however, depends heavily on accurate impedance matching and controlled interconnect parameters. Mismatched impedances can create reflections and signal distortion, undermining timing precision. Therefore, maintaining a uniform characteristic impedance (Z_0) across all branches is essential. The design process must also consider the physical implementation—dielectric materials, conductor thickness, and routing layers all affect delay and attenuation.

In this project, an H-Tree clock distribution network is designed, modeled, and simulated using Keysight Advanced Design System (ADS) and its LineCalc utility. The primary goal is to achieve minimal clock skew across a 16-leaf network operating at 1 GHz. Two models are constructed: an ideal transmission line (TLIN) network ignoring losses, and a physical model using microstrip (MLIN) and stripline (SLIN) interconnects that incorporate conductor and dielectric loss. The design follows the geometric and electrical constraints provided in the course specifications, including a $9 \mu\text{m}$ copper thickness, a minimum dielectric thickness of $54 \mu\text{m}$, and a 45Ω target impedance.

Simulation results confirm that the H-Tree provides nearly identical propagation delays to all leaves, with less than 12 ps skew in the physical model and negligible skew in the ideal case. These results validate the symmetry and impedance-matching principles of the H-Tree as an effective structure for high-frequency clock distribution networks.

II. DESIGN AND PROCEDURE OF H-TREE IDEAL USING IDEAL TRANSMISSION LINE MODEL

The design of the H-Tree clock distribution network follows a step-by-step methodology to ensure electrical balance and symmetry across all sixteen output terminals. The overall process involves (1) defining design parameters and electrical constraints, (2) determining interconnect geometries using LineCalc, and (3) implementing and simulating both ideal and physical network models within ADS.

A. Parameter Specification

The H-Tree network was designed for a 1 GHz operating frequency with a 5 V source and 0.1 ns rise/fall time. The package cross-section consists of four metal layers: Metal 1A (VDD), Metal 2A (signal – stripline), Metal 3A (ground plane), and Metal 4A (signal – microstrip). Copper thickness was set to $9 \mu\text{m}$, and the dielectric layer was $54 \mu\text{m}$ thick, corresponding to the minimum process specification. The dielectric material has a relative permittivity (ϵ_r) of 3.5.

Table 1. Design Specifications

Parameter	Symbol	Value
Source Voltage	V_s	5V
Frequency	f	1 GHz
Rise/Fall time	tr/tf	0.1ns
Dielectric Constant	ϵ_r	3.5
Conductor Thickness	t	$9 \mu\text{m}$
Dielectric Height	h	$54 \mu\text{m}$
Target Impedance	Z_0	45Ω

Simulation of the ideal H-Tree produced perfectly balanced propagation paths. All output waveforms reached the logic threshold simultaneously, confirming the zero-skew behavior expected from a symmetrical H-Tree

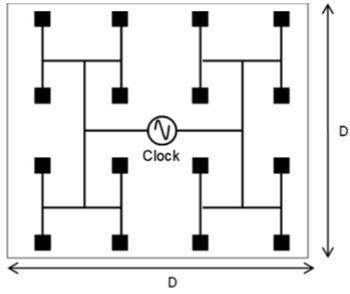


Figure 1: Clock Tree Distribution Schematic

B. Impedance Matching Using LineCalc

LineCalc was used to compute the interconnect widths required to achieve a characteristic impedance of 45Ω for both microstrip and stripline configurations. For the given dielectric height and copper thickness, the required trace width was approximately 6 mils. Adjusting the dielectric height slightly within tolerance allowed fine-tuning of the impedance for optimal matching with the driver and terminations.



Figure 2. Stripline ADS Synthesis

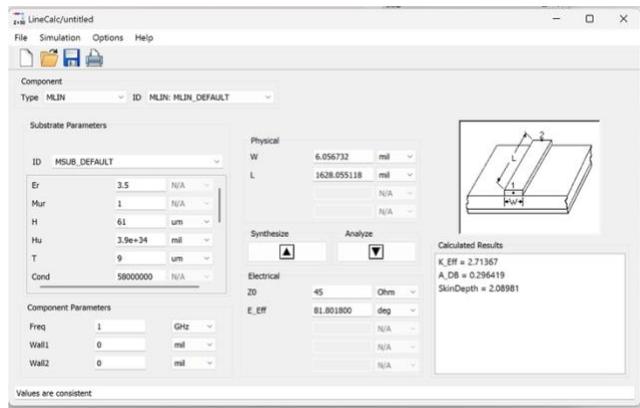


Figure 3. Microstrip Line ADS Synthesis

III. Ideal H-Tree Model (Lossless)

The initial H-Tree design was modeled using ADS TLIN components, representing ideal lossless transmission lines. The network consisted of four branching levels, yielding sixteen output nodes. Each leaf was terminated with a 45Ω resistor to match the characteristic impedance of the interconnects. The Thevenin equivalent driver was modeled using a 5 V pulse source with a 45Ω source resistance.

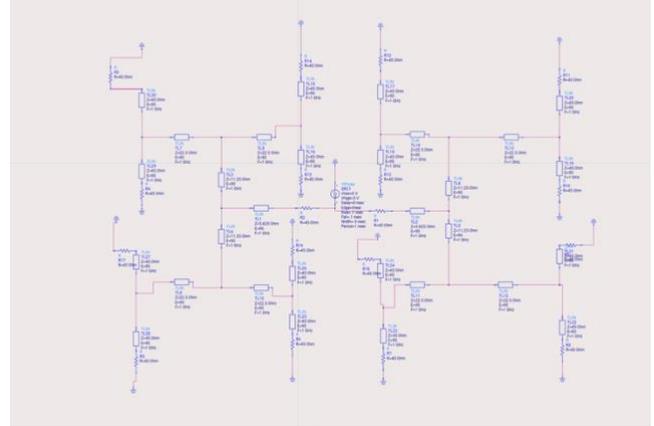


Figure 4. ADS Schematic of Ideal H-Tree

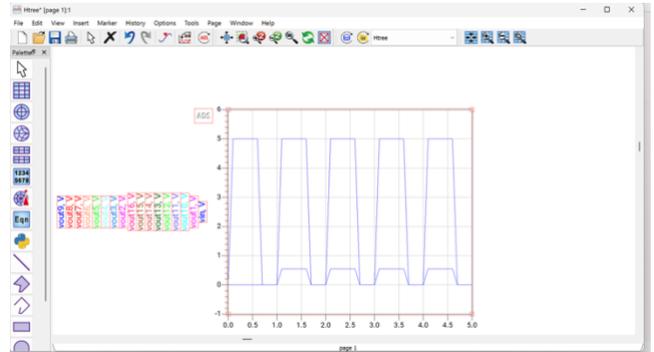


Figure 5. Voltage waveform at the input and 16 nodes at branch 4 in an ideal representation of Transmission lines.

TABLE II
H-TREE PARAMETERS FOR IDEAL TRANSMISSION LINE MODEL

Transmission Lines	Impedance (Z_0)	Length of Tline (L)	Electrical Length (E)
Branch 4	45Ω	7.5 mm	90 degrees
Branch 3	22.5Ω	7.5 mm	90 degrees
Branch 2	11.25Ω	15 mm	90 degrees
Branch 1	5.625Ω	15 mm	90 degrees

IV. PHYSICAL MODEL USING MICROSTRIP AND STRIPLINE

To incorporate real-world losses, a physical model of the H-Tree was developed using MLIN and SLIN components. These elements included conductor loss, dielectric loss, and dispersion effects.

A. Substrate Definition

Two substrates were defined in ADS:

- MSUB (Microstrip): $h = 54 \mu\text{m}$, $t = 9 \mu\text{m}$, $\epsilon_r = 3.5$, $\tan\delta = 0.025$
- SSUB (Stripline): $b = 255 \mu\text{m}$ (distance between planes), $t = 9 \mu\text{m}$, $\epsilon_r = 3.5$, $\tan\delta = 0.025$

Microstrip lines were routed on the top layer (Metal 4A), while stripline segments were used on internal signal layers (Metal 2A), ensuring orthogonal routing between layers.

TABLE III
H-TREE PARAMETERS FOR MICROSTRIP AND STRIPLINE TRANSMISSION
LINE MODEL

Parameter	Branch 4 (MLIN)	Branch 3 (SLIN)	Branch 2 (MLIN)	Branch 1 (SLIN)
Impedance (Z_0)	45 Ω	22.5 Ω	11.25 Ω	5.625 Ω
Electrical Length (E)	90 deg	90 deg	90 deg	90 deg
Line Length (L)	7.5 mm	7.5 mm	15 mm	15 mm
Line Width (W)	6.06 mil	12.8 mil	37.3 mil	62 mil
Dielectric thickness	54 μm	255 μm	54 μm	255 μm

B. Simulation Results

Transient analysis of the physical H-Tree revealed slightly attenuated signals compared to the ideal model. The maximum voltage amplitude at the outputs decreased to ~ 1.7 V due to resistive and dielectric losses, while the overall propagation delay increased to approximately 1.31 ns. Despite these losses, the maximum skew between the earliest and latest outputs remained below 12 ps, demonstrating the continued symmetry of the structure.

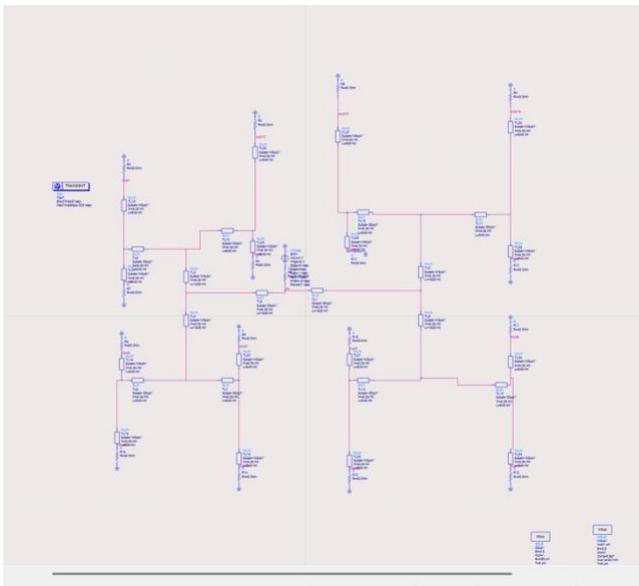


Figure 6. ADS schematic of physical H-Tree

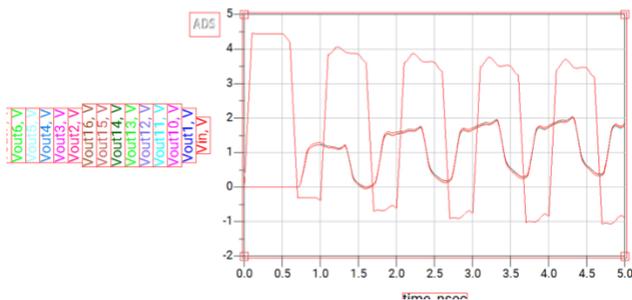


Figure 7. Output waveforms for MLIN/SLIN model

V. RESULTS AND ANALYSIS

Table 4 compares the electrical performance of the ideal and physical models. The data confirms that the H-Tree topology maintains near-zero skew even when realistic losses are introduced. The physical implementation shows slightly reduced voltage levels and longer propagation times due to parasitic effects, but these variations remain within acceptable design tolerances.

Model	Peak Voltage (V)	Delay (ns)	Skew (ps)	Observation
Ideal (TLIN)	5	1.25	<5	Perfect Symmetry, zero loss
Physical (MLIN/SLIN)	1.7	1.31	8-12	Small Attenuation, minimal skew

The physical model's reduced amplitude and minor delay shift illustrate the impact of conductor and dielectric loss, yet the structure remains effective for balanced timing distribution.

VI. Conclusion

The H-Tree clock distribution network designed and simulated in this project successfully achieved low-skew signal distribution across sixteen endpoints. The LineCalc-based impedance synthesis ensured uniform transmission characteristics, and ADS simulation verified minimal timing differences across all leaves. While attenuation and delay were observed in the physical model, the network's symmetry preserved synchronization integrity.

This experiment validates the H-Tree as an optimal structure for high-speed, low-skew clock distribution within multi-layer integrated packages.

REFERENCES

- [1] Keysight Technologies, *ADS LineCalc and Transmission Line Models User Guide*, 2023.
- [2] EE 310 Lecture 13_2, *Clock Distribution Layout & Simulation*, 2024.