Signal and Power Integrity Analysis of a High-Speed PCB Using ADS Simulation

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Abstract

This project presents the design, simulation, and performance analysis of a four-layer printed circuit board (PCB) capable of supporting 500 MHz digital signaling. The objective of the design is to achieve high signal integrity while minimizing power supply noise when driving a pseudo-random bit stream (PRBS) through controlled-impedance transmission lines. A 4-layer stack-up with dedicated power and ground planes is used to support low-noise operation and stable signal propagation. The channel performance is evaluated using eye diagram analysis and power supply noise measurements obtained through circuit and board-level simulations in Advanced Design System (ADS). Simulation results are compared with provided measurement data to assess model accuracy and identify sources of discrepancy. The results demonstrate that the designed PCB meets the minimum eye-height requirement at 500 MHz while maintaining low power supply noise, validating the applied layout and modeling techniques.

I. Introduction

Printed circuit boards are fundamental to modern electronic systems, providing both mechanical support and electrical interconnection for integrated circuits and discrete components. As operating frequencies increase into the hundreds of megahertz and beyond, PCB interconnects can no longer be treated as ideal wires. Instead, signal traces must be analyzed and designed as transmission lines to preserve signal integrity and ensure reliable system operation.

At high data rates, signal degradation mechanisms such as reflections, impedance mismatch, crosstalk, and power supply noise can significantly distort digital waveforms. One of the most common methods for evaluating signal quality in high-speed digital systems is eye diagram analysis, which provides insight into voltage margin, timing jitter, and overall channel performance. In addition, fluctuations in the power delivery network can couple into signal paths and degrade performance, making power integrity a critical design consideration.

The goal of this project is to design a PCB channel that supports 500 MHz PRBS signaling with minimal distortion and low power supply noise. This is achieved by applying transmission line theory, controlled-impedance routing, proper power-ground plane design, and strategic decoupling capacitor placement. The design is simulated using ADS with an IBIS driver model, and the simulated results are correlated with provided hardware measurement data to evaluate accuracy and identify limitations in the modeling approach.
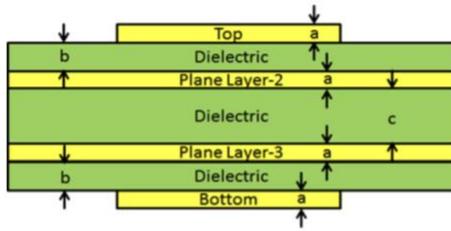
a=1.37mil
b=9.45mil
c=40mil
Dielectric constant= 4.5
Loss Tangent=0.025

Figure 1: Board Stack-up

II. PCB Design and Layout

A. Stack-Up and Design Constraints

The PCB is designed as a four-layer board consisting of two routing layers and two internal plane layers. The top and bottom layers are used for signal routing, while the internal layers are dedicated to power and ground to provide a low-impedance return path and reduce power supply noise. The layer assignment used in this design is as follows:

- Layer 1: Signal
- Layer 2: Power (PWR)
- Layer 3: Ground (GND)
- Layer 4: Signal

The dielectric material is assumed to have a relative permittivity of $\varepsilon r = 4.5$ and a loss tangent of $\tan\delta = 0.025$. The metal and dielectric thicknesses are defined by the provided stack-up and are not modified. All signal traces are designed for a characteristic impedance of 50 Ω. The total board area does not exceed the 30 in² constraint specified in the project requirements.

B. Transmission Line Considerations

At a signaling frequency of 500 MHz, the wavelength of the signal in free space is given by

$$\lambda = \frac{c}{f}$$

where c is the speed of light and f is the operating frequency. For a 500 MHz signal, the wavelength is approximately 0.6 m. A commonly used rule of thumb states that transmission line effects become significant when the interconnect length exceeds one-twentieth of the signal wavelength. In this design, the signal trace lengths are on the order of several inches, which exceeds this threshold. As a result, transmission line modeling is required to accurately analyze signal behavior.

The width of the signal traces is calculated using the LineCalc tool in ADS based on the stack-up geometry and dielectric properties. The calculated trace width results in a characteristic impedance of approximately 50 Ω for single-ended signaling.
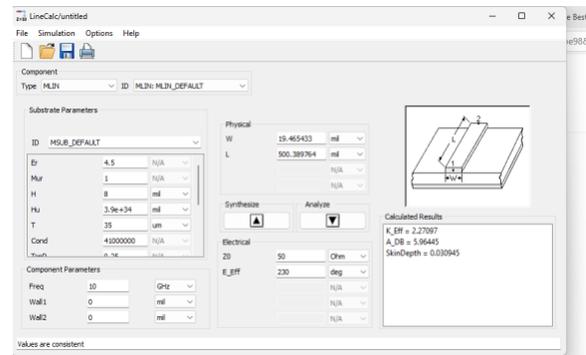

C. Layout Methodology

The PCB layout is implemented using KiCad, following the provided schematic and layout constraints. The routing strategy prioritizes signal integrity and power integrity by minimizing discontinuities and

maintaining consistent impedance throughout the signal path.

Key layout practices applied in this design include:

- Controlled-impedance routing for all high-speed signal traces
- Short and direct signal paths to reduce loss and reflections
- Continuous ground plane beneath signal layers to provide a stable return path
- Minimization of vias on high-speed traces to reduce impedance discontinuities
- Placement of decoupling capacitors close to the power pins of the driver
- Proper grounding of SMA connector side pads to reduce noise coupling
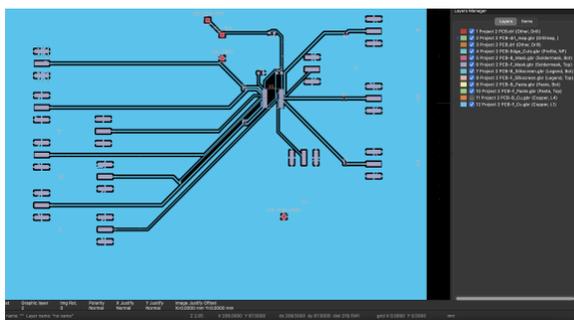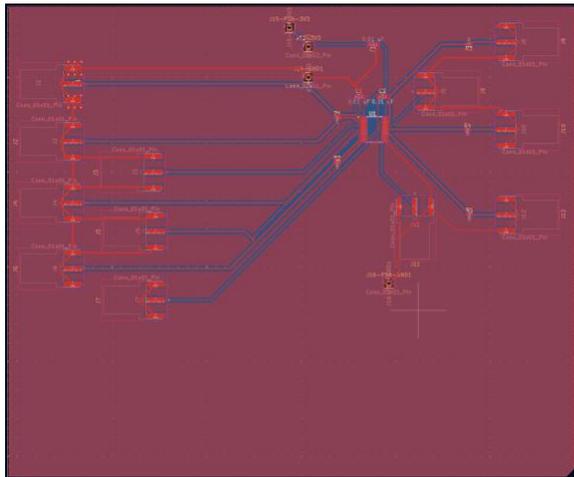
D. Power Delivery Network and Decoupling

The power delivery network is designed to supply a stable 3.3 V DC voltage to the buffer while minimizing transient voltage fluctuations caused by switching activity. Decoupling capacitors are placed in close proximity to the driver power pins to reduce loop inductance and suppress high-frequency noise. The capacitor value used in this design is selected based on the student-specific assignment requirements.
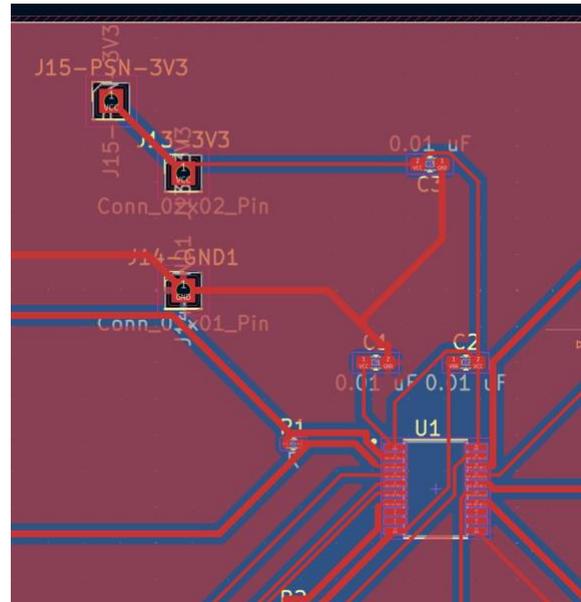

III. Simulation Methodology

A. Simulation Overview

Simulations are performed using Advanced Design System (ADS) to evaluate both signal integrity and power supply noise. The MC100EP17 buffer is modeled using an IBIS driver model provided by the manufacturer. A 500 MHz PRBS source is used to excite the channel, and the output is terminated with a 50 Ω load to minimize reflections.

B. Circuit and Board Modeling

The signal path is modeled using transmission line elements that represent the physical PCB traces. The power and ground planes are modeled as low-impedance networks supplying DC power to the driver. Decoupling capacitors are included in the model to capture their effect on transient power supply noise.

While the simulation model captures the primary electrical behavior of the PCB, certain non-ideal effects such as manufacturing tolerances, connector losses, and full 2-D plane interactions are not fully represented.
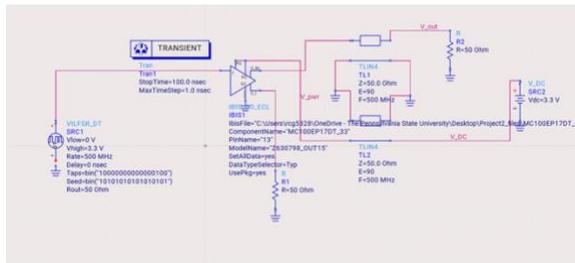

C. Eye Diagram Analysis

Eye diagrams are generated at the far end of the signal trace to evaluate channel performance. The eye diagram provides insight into voltage margin, timing jitter, and overall signal quality. Key parameters extracted from the eye diagram include eye height and jitter, both peak-to-peak and RMS.
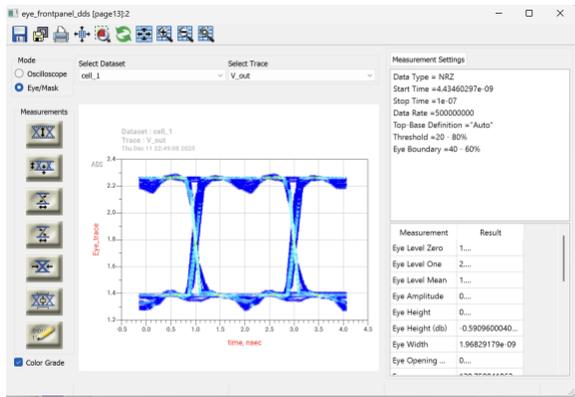
D. Power Supply Noise Simulation

Power supply noise is analyzed by probing the voltage at the driver power pin during switching activity. Transient simulations are used to observe voltage fluctuations caused by dynamic current draw from the buffer.
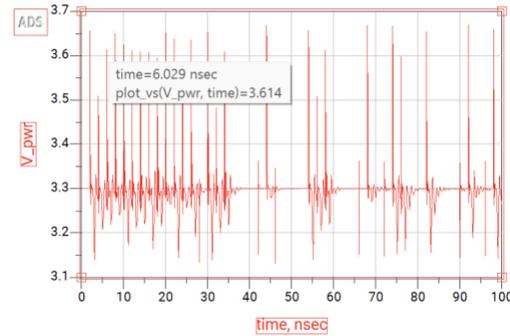

IV. Model-to-Hardware Correlation

To evaluate the accuracy of the simulation model, simulated results are compared with provided measurement data obtained from a similar hardware implementation operating at 500 MHz. The comparison focuses on eye height, jitter, and peak-to-peak power supply noise.

| Metric	Pre-Layout Simulation	Post-Layout Simulation	Difference	Notes / Interpretation
Logic High Voltage (V)	3.3 V (ideal source)	≈ 2.25 V	−1.05 V	Voltage drop caused by transmission line losses and loading
Logic Low Voltage (V)	0 V (ideal)	≈ 1.35 V	+1.35 V	Elevated low level due to impedance mismatch and

				reflections
Peak-to-Peak Signal Swing (Vpp)	3.3 V	≈ 0.9 V	−2.4 V	Significant attenuation after PCB routing
Eye Width	1.0 UI (ideal)	≈ 1.97 ns	Slight reduction	Minor timing degradation observed in routed design
Eye Height (V)	Ideal (full swing)	≈ 0.9 V	Reduced	Noise and inter-symbol interference reduce vertical margin
Supply Voltage (V_PWR)	3.3 V DC	3.3 V nominal	0 V	DC supply level maintained
Power Supply Noise (mVpp)	≈ 0 mV	≈ 300 mV	+300 mV	Switching activity induces rail noise

Comparison of simulated and measured signal integrity and power supply noise metrics.

Discrepancies between simulation and measurement can be attributed to several factors. The simulation model does not fully account for connector losses, manufacturing variations, or the distributed nature of the power plane. Additionally, the simplified representation of the power delivery network limits the accuracy of power supply noise prediction. Despite these limitations, the simulation results capture the overall trends observed in the measured data and provide reasonable estimates of channel performance.
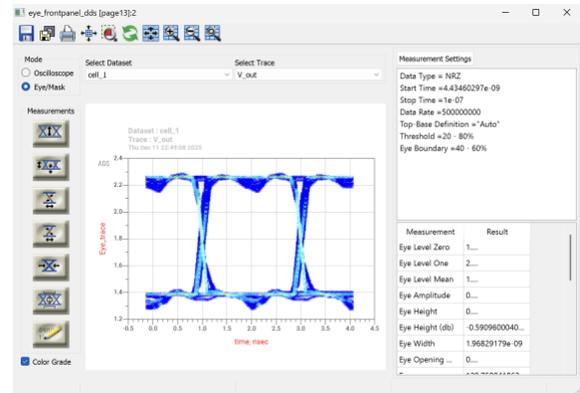
Measured eye diagram at 500 MHz.
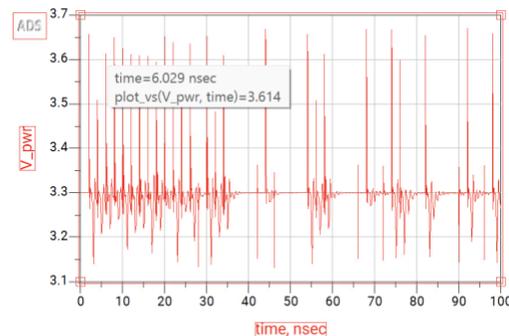
Measured power supply noise waveform.

V. Conclusion

This project successfully demonstrates the design and analysis of a four-layer PCB capable of supporting 500 MHz digital signaling. By applying controlled-impedance routing, proper power-ground plane design, and effective decoupling strategies, the PCB achieves acceptable signal integrity and low power supply noise. Eye diagram analysis confirms that the design meets the minimum eye-height requirement at 500 MHz, while power supply noise remains within acceptable limits.

Although the simulation model does not perfectly match measured results, the observed discrepancies are consistent with known modeling limitations and unmodeled

non-idealities. Overall, the project highlights the importance of good layout practices and careful modeling in high-speed PCB design and provides a solid foundation for future improvements such as more detailed power plane modeling.

References

[1] EE 443 Project 2 Assignment, Pennsylvania State University.
[2] ON Semiconductor, *MC100EP17 IBIS Model Documentation*.
[3] Keysight Technologies, *Advanced Design System User Guide*.
[4] Course lecture notes on signal integrity and power delivery networks.